A 9.5 GHz Commercially Available 1/4 GaAs Dynamic Prescaler with Suppressed Noise Performance

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ABSTRACT

A mass-production level 1/4 GaAs monolithic dynamic prescaler operating at a single clock input of 9.5 GHz with a power dissipation of 450 mW has been successfully realized. In addition, the phase noise performances were also investigated to obtain an excellent result and to accomplish the verified level of -100 dBc/Hz and -120 dBc/Hz at 100Hz and 10 KHz offsets for a 6.725 GHz input, which are considered to be low enough for a practical use.

I INTRODUCTION

Ever since the first emerge of the technical work in 1974[1], the GaAs IC devices have advanced step by step by acquiring and mastering the state-of-the-art technologies of the times during these one and a half decades. Recently, the reliability assessment report on the GaAs IC devices has been introduced by Katsukawa et al[2], which offers us a promising foresight that they will possibly have a high potentiality of being accepted in the actual market in near future.

On the other hand, many systems, especially in the microwave and gigabit fields, are strongly required from the environmental needs to meet the following improvements such as; (1) higher frequency or speed performance, (2) lower noise characteristic, (3) less or tuning free feasibility and (4) more compact size or lighter weight, in order to pursue much higher quality or performance and much lower cost for the future system. From these points of view, the GaAs IC devices are expected to play a substantial role in the field applications of microwave equipments and high speed instruments.

This paper will describe a 1/4 GaAs monolithic dynamic prescaler suitable for PLL(Phase Locked Loop) circuit in microwave communication and measurement systems. The developed unit can operate single clocked at a maximum frequency of 9.5 GHz under a single or a dual power supply conditions. The power dissipation is as small as 450 mW with an output power of more than + 0 dBm, large enough to drive any GaAs or Si bipolar high speed prescaler. In Chapter II, the circuit design and simulation will be discussed. Then, in Chapter III will be given a brief explanation of the bacic FET and the fabrication process, and in Chapter IV, experimental results including phase noise characteristics will be reported. Finally, a conclusion will be given in Chapter V.

II DESIGNING

When making a comparison between dynamic[3] [4] and static prescalers, the dynamic one has the following advantages over the static one;
(1) dynamic prescaler is about two times faster in operation than the static one when the same FETs are used.
(2) device complexity of the dynamic prescaler is about one thirds smaller than that of the static one, which might lead to a easy fabrication and therefore a high process yield.

With the dynamic prescaler, however, there is a disadvantage that the lower end of the operating frequency range is limited at around 1~2 GHz due to a current leakage in the transfer gate FET[3].

(A) Circuit Design

Fig.1 shows a block diagram for the developed dynamic prescaler, consisting of two basic 1/2 prescaler blocks constructed with a BFL(Buffered FET Logic) circuit. The block includes both an inverter and a buffer amplifier, which can permit practical single clock operation and direct cascaded configuration. The circuit design was carried out by using a SPICE simulation program. The based FET has characteristics such as a threshold voltage(Vt) of -1.0 V and a gate propagation delay time (Tpd) of 55 ps. Fig.7 shows a relationship between Vt and Tpd obtained from a 15-stage ring oscillator. With a decreasing Vt (becoming a deeper Vt), Tpd monotonically decreases to saturate where Vt is reached at around -1.0 V. The dynamic prescaler bears a certain similarity in operation to the ring oscillator, and this suggests that Vt of -1.0 V be the most suitable selection from view point of the speed and power dissipation.

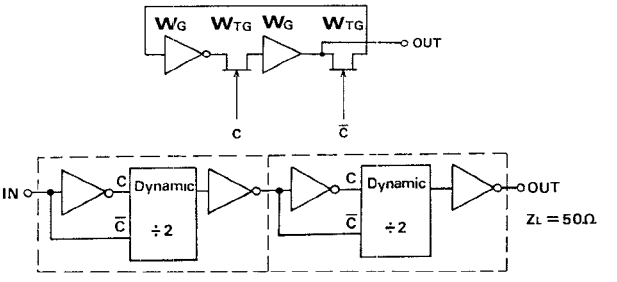

Fig.1 The prescaler block diagram is composed with two 1/2 prescalers. A complementary clock is generated by an inverter at the input.

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As for a FET size, the gate width(Wg) in the inverter and the buffer portion in Fig.1 is one of the dominant factors determining the operation speed for the dynamic prescaler. According to the computer simulation with interconnect stray capacitances taken into consideration, over 60 um of FET has little influence on the speed improvement mainly due to the fan-out loading effect. Based on the result, the gate width was decided to be 50 um for the first and 30 um for the second 1/2 stage, respectively, through the speed and power optimization.

Then, the transfer gate FET size(Wtg) is another important factor that defines the operating frequency range. Fig.2 shows how the maximum and minimum operating frequency(Fmax,Fmin) varies when Wtg changes. As can be seen in the figure, Fmin drastically degrades when Wtg is over 40 um, and on the contrary, Fmax almost remains constant. Wtg was finally designed to be 30 um and 10 um for the first and the second stage 1/2 prescalers so that the maximum operating frequency range could be obtained with an allowable amount of Fmax deterioration.

(B) Layouting

Close attention has been paid not to layout the IC circuit elements too near to have an undesired leakage current increase. In addition, interconnection including MIM capacitors and FET gate pads has been formed on the dielectric films such as SiO_2 or Si_3N_4, not directly on the surface of a GaAs substrate, so as to prevent the side gating effect[5] or some extrinsic low frequency oscillation phenomena[6][7][8] from being brought about through the GaAs semi-insulating substrate. A chip photograph is shown in Fig.3, and a chip size is 1.1 x 1.2 mm^2.

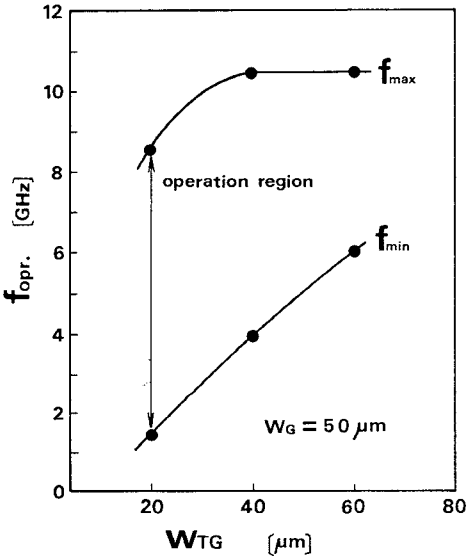


Fig.2 1/2 prescaler Fmax and Fmin dependencies on Wtg. The gate width defines the operating frequency range.

III FABRICATION

The fundamental FET used in the prescaler has a T-shaped offset gate of WSi refractory metal with TiN/Pt/Au on top for reducing a gate resistance. Fig.4 shows a cross sectional view of the FET. The gate length is around 0.8 um. Si^+ ion-implantation was used to make the active layers for FETs, diodes, and resistors as well as the n^+ layers beneath the ohmic electrodes. The FET Vt was chosen to be about -1.0 V with a transconductance (Gmo) of 170 mS/mm. Dry etching was utilized in the gate-slit windowing and through-hole opening. Tripple layer wiring of Au was realized by using ion-milling and planarization techniques.

IV EXPERIMENTAL RESULTS

(A) RF Performance

Fig.5 shows surface-mount type, harmetic sealed, 8 pin ceramic packages for the 1/4 and 1/2 prescalers. RF measurements were made by mounting the packaged prescaler on a house-made RF jig. Fig.6 shows input sensitivity versus frequency characteristics at different temperatures together

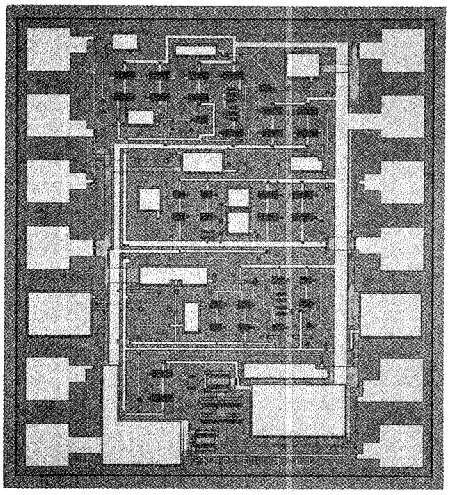


Fig.3 Chip photograph of the developed prescaler in which about 60 elements are integrated. A chip size is 1.1x1.2 mm^2

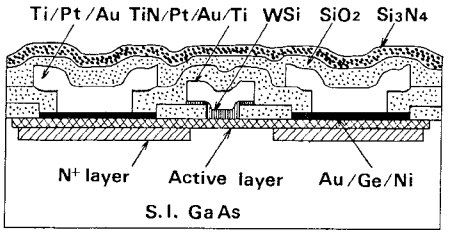


Fig.4 A cross sectional view of the Fundamental FET. WSi refractory metal was used for a gate. The gate length is around 0.8 um.

with output power behaviors. The unit exhibited a wide frequency range of operation from 2.4 to 9.6 GHz, nearly two octaves, at an input power level of + 10 dBm at room temperature.

Meanwhile, an output power was weakly dependent on the frequency throughout the range. However, it did not change more than 1 dB and resulted in +1.3 dBm at 9.5 GHz as well as +2 dBm at 8 GHz. At a high temperature of 75°C, Fmax slightly decreased to 9.1 GHz with a temperature coefficient of -10 MHz/°C for such a simple configuration without any temperature compensation circuit. On the other hand, Fmin almost remained constant except at a lower input power level.

Fig.7 shows an Fmax dependency on Vt over several wafer process lots, with that of ring oscillator Tpds superimposed on it. It can be seen in the figure that even less increase in Fmax would be expected when Vt exceeds over -1.0 V. This would confirm the validity in the circuit optimization put into practice for the dynamic prescaler. Fig.8 shows Fmax and Fmin distrtibutions within a wafer, evaluated by on-wafer RF proving technique. Sharply high peaks indicate a fairly good uniformity of operation, and it possibly promises a high operation yield. Fig.9 shows the dynamic prescaler output in the forms of time and frequency domains. Stable operation and about 20 dB D/U signal ratio have been observed.

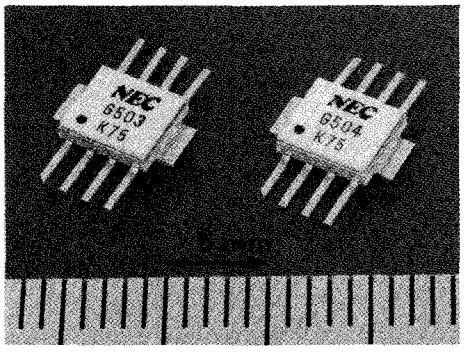
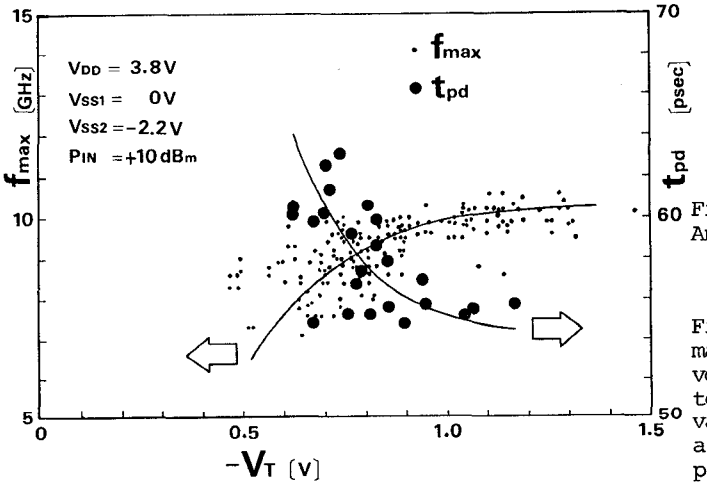
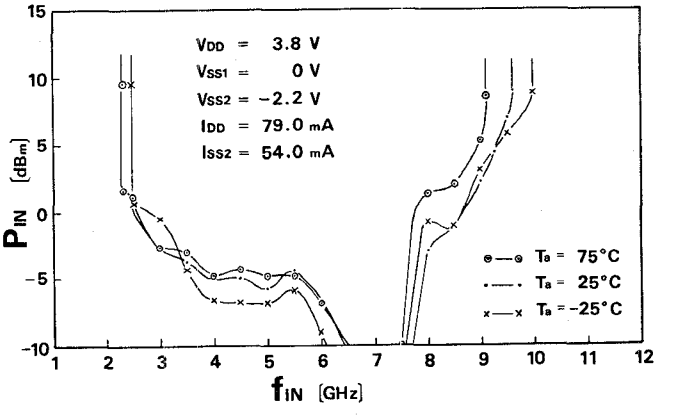


Fig.5 The surface-mount type, harmetic sealed, 8 pin ceramic packages; for 1/4 prescaler on left and 1/2 prescaler on right.





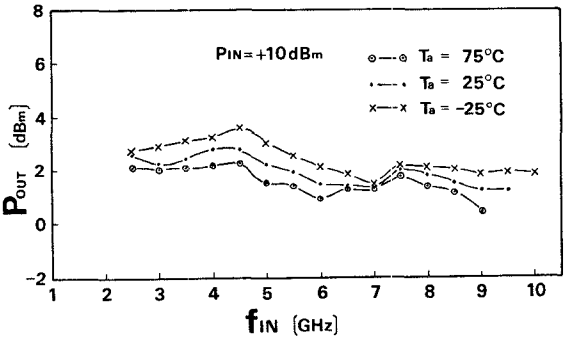


Fig.6 Input sensitivity characteristics at three different temperatures of -25, +25 and +75°C. The relations between the output power and the frequency are also shown. The bias condition are; Vdd=3.8V,Vss1=0V,Vss2=-2.2V,Idd=79mA and Iss=54mA.

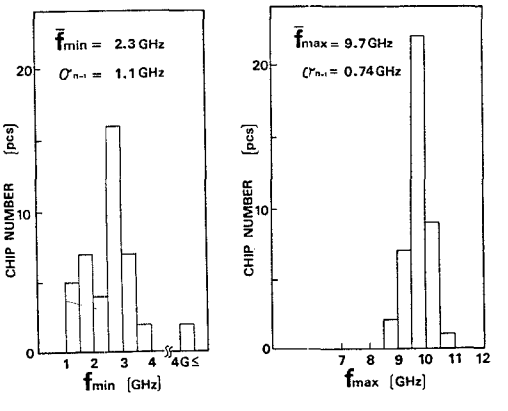


Fig.8 Fmax and Fmin distributions within a wafer. An Fmax of 9.7 GHz is realized on a average.

Fig.7 This shows a relationship between the maximumfrequency(Fmax) and the FET threshold voltage(Vt). Fmax tends to increase in proportion to Vt and to saturate around at Vt=-1.0V. The values of gate propagation delay time(Tpd) based on a 15-stage ring oscillator performance is also plotted.

(B) Phase Noise Performance And Reliability

The prescaler phase noise is one of the importannt factors to be evaluated when considering practical system applications. Fig.10 shows phase noise performances of the dynamic prescaler, obtained by making use of an HP 3048A phase noise measurement system. Curve A is a noise curve of a signal source, for which in-house high purity APC (Automatic Phase Controlled) oscillator was utilized at Fosc=6.725 GHz, for the purpose of preventing the prescaler noise level from being covered with the source noise and consequently an accurate investigation from being made impossible. Curve B represents an output noise curve of the 1/4 prescaler unit. As clearly seen in the figure, curve A can be completely overlapped on curve B by the 12 dB noise level reduction. This is because the prescaler reduces the sideband noise level by 20log 1/4=-12 dB, meaning that the prescaler perfectly works without producing any fatal noise throughout the frequency offset range of 1 Hz to 100 KHz. The carrier signal frequency of 6.725 GHz is the highest of all ever reported.

Furthermore, the phase noise behaviors at -30°C and +75°C were also investigated and shown in Fig.11. There was no anomalous noise peak generated across the band of interest, and it should be noticed that the noise level verifications of -100 dBc/Hz and -120 dBc/Hz have been accomplished at 100 Hz and 10 KHz offsets, respectively, at a high frequency of 6.725 GHz.

Then, taking into consideration an actual PLL system set-up, the prescaler unit was directly connected to an oscillator with a shunt 50 ohm resistor. The total output noise of the oscillator was measured by a linear detector and a base band spectrum analyzer for a 6.85 GHz input. Fig.12 shows the obtained results in comparison with a 50 ohm termination only. The noise performance hardly deteriorated in spite of an oscillator high sensitivity to external loading.

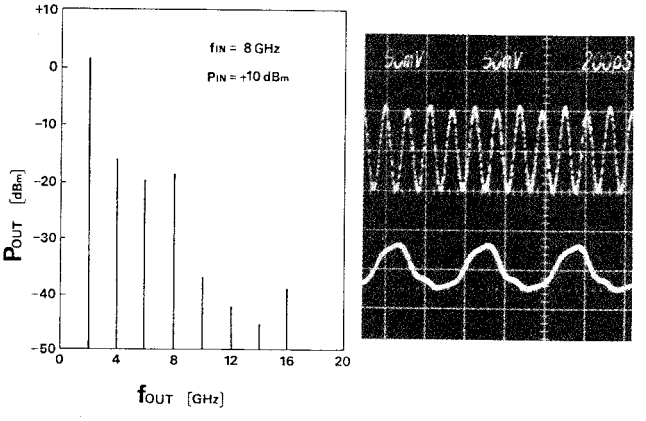


Fig.9 Operating waveforms at Fin=9GHz and divided-by-4 output frequency spectrum at Fin=8GHz are shown. The bias conditions are as follows; Vdd=3.8V,Vss=-2.2V,Pin=+8dBm. 20 dB ATTs are used at both input and output.

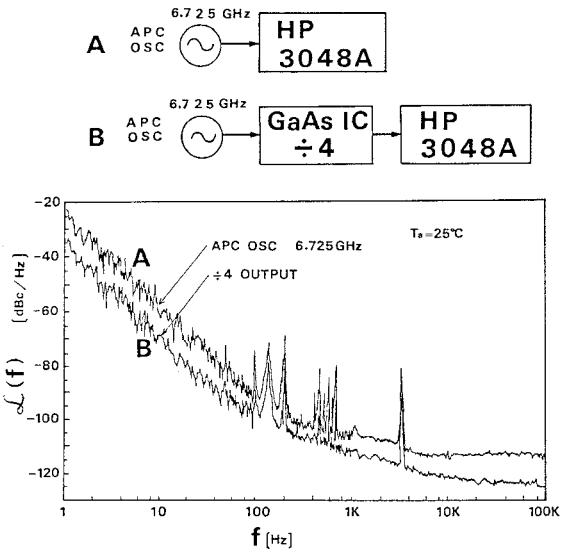


Fig.10 A phase noise performance of the prescaler. An high purity oscillator of 6.725 GHz was employed as a signal source to the prescaler unit. The input A and output B noises of the unit were measured by an HP phase noise measurement system. The noise level was expectedly reduced by 12 dB without any anomalous noise peak. Consequently, for instance, -120 dBc/Hz level could be discussed at a 10 KHz offset.

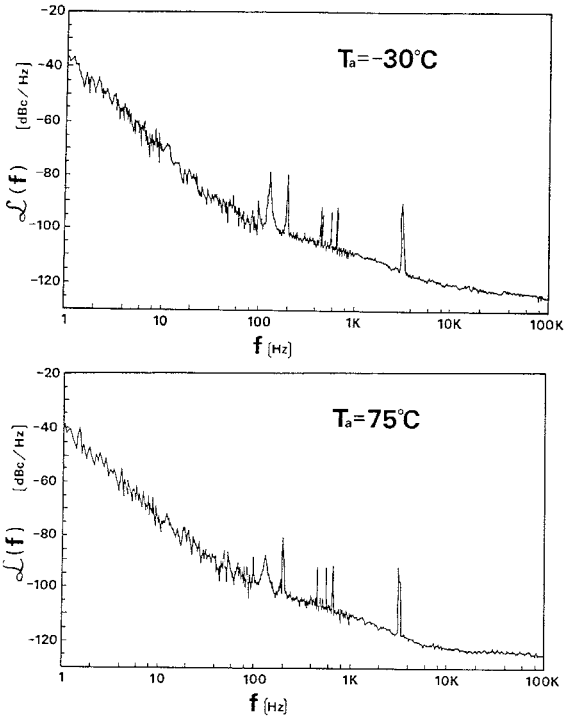


Fig.11 The phase noise temperature dependence. The measurements were made at -30,25 and 75°C. The noise hardly varied within this temperature range.

The reliability is a final scale-measure to the degree of the product completeness. Fig.13 shows the RF burn-in testing results for the prescaler at a device junction temperature(Tj) of 115°C. Fmax changes only a few percent over 3000 hours without any failure, meaning that the reliability potential is large enough just like that of the S-band two stage amplifier reported previously[2].

V CONCLUSION

In conclusion, a single-clocked dynamic 1/4 prescaler, operating at 9.5 GHz with high yields and stability, could be realized using the WSi offset gate FET due to circuit simplicity and design refinement. Besides, the superior noise performance was also achieved in the wide frequency offset range. The various results botained so far will possibly give us a breakthrough to commercial availability of the ultra high speed GaAs prescaler.

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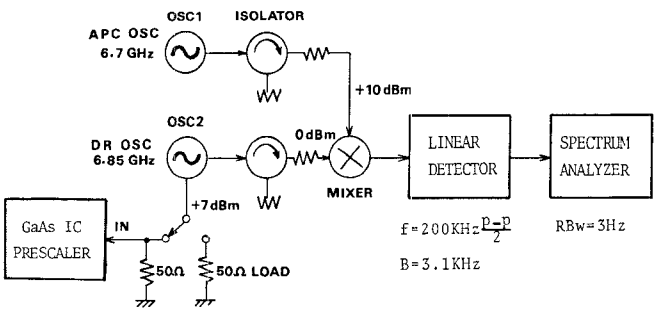

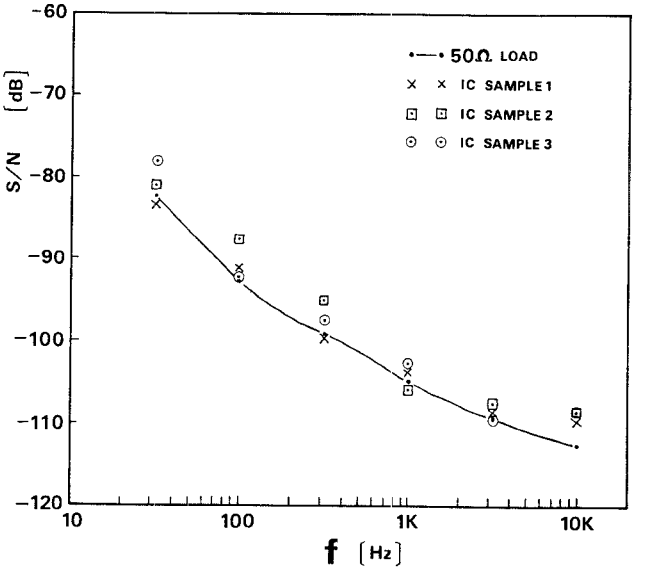

Fig.12 A block diagram for an oscillator S/N measurement set-up. The prescaler was directly connected to the oscillator 2 with a shunt 50 ohm resistor. S/N data of three different prescaler units are plotted in up to 10 KHz offset range with a result of a 50 ohm termination only for a reference.

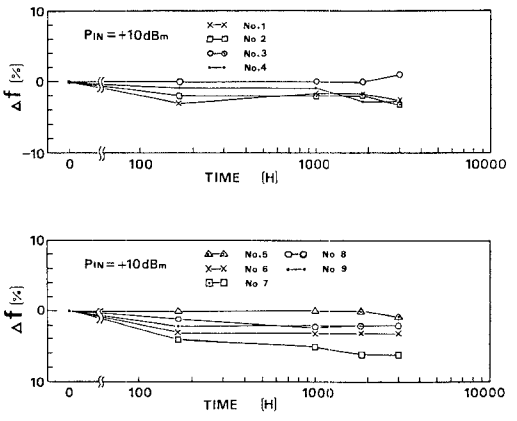

Fig.13 RF burn-in testing was fulfilled for the prescaler at a device junction temperature(Tj) of 115°C. There is no failure over 3000 hours.